PRECISION DEVICES knowles

BUILD-TO-PRINT BASICS EBOOK

A COMPREHENSIVE GUIDE TO KNOWLES PRECISION DEVICES' BUILD-TO-PRINT SERVICES AND THIN-FILM TECHNOLOGY

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INTRODUCTION

At Knowles Precision Devices, we are not trying to be your typical commodity component manufacturer. We want to do things that are hard and help customers solve their most difficult engineering challenges. This is why over the past three decades we have focused on manufacturing high-frequency, high Q components that can function reliably, even in the most demanding applications. Additionally, since every application has different needs, we offer a wide-variety of off-the-shelf catalog solutions, build-to-print services, and even the ability to work closely with customers to create custom thin-film solutions.

The marriage of ceramic expertise, manufacturing know-how, product quality, customer service, product customization, and clever microwave and RF design engineering allows us to offer this variety, while many of our competitors cannot. To provide a better understanding of our build-to-print services in general and the breadth of our offerings, as well as how our thin-film technology can benefit your applications, we've put together this Build-to-Print Basics eBook.

Our Approach to Build-to-Print

Our build-to-print process typically starts with a customer providing us with circuit drawings or schematics. We then use those documents to produce a portion of the circuit to spec using the most appropriate materials (we can also provide much higher levels of service and consultation for custom options, which we will discuss later). Typical applications we service with build-to-print include the following:

- Heat sinks and standoff
- Integrated passive devices
- Custom resistor capacitor networks
- Lange couplers and power combiners
- Electromagnetic interference (EMI) filters
- High-frequency filters
- Microwave integrated circuits (MIC)
- Bias decoupling and filtering
- Lumped element impedance matching networks
- PA stabilizations
- Impedance matching and power combining networks

A Brief Overview of Thin Film

At a high level, thin film is a layer of material used to fabricate electronic components that generally ranges from fractions of a nanometer to several micrometers in thickness. Constructing circuits using thin film offers several advantages over other techniques, including the high-precision patterning that can be reached and the ability to make components much more compact versus other material options. This makes thin film a particularly good material choice for high-frequency RF devices where precision and accuracy are essential.

Knowles Precision Devices provides custom ceramics for thin-film development that offer significantly better thermal performance than most industry-standard ceramics. Our thin-film substrates also offer a sufficiently higher dielectric constant (K), which is ideal for miniaturization and temperature-stable performance.

Custom Solutions for Complex Designs

When working with customers to build custom thin-film solutions, we can offer as much, or as little, support as needed. This can range from simply having one of our engineers look at spec drawings to see what areas of the design can be improved upon to us working together with a customer to create a unique design. Customers who want to work with us to build to specification can contact us to discuss your specific application requirements.

In addition to offering our engineering expertise to help customers develop the most efficient and effective designs, we offer a wide variety of substrates to ensure the final component can meet your exact needs. Beyond working with standard substrates such as polished alumina, we have more than one hundred proprietary and/or patented ceramic formulations that offer significantly better thermal performance than the majority of industry-standard ceramics. Table 1 highlights the performance characteristics of both the

standard substrates and some of the custom dielectric materials we build devices on.

Table 1 Substrate Performance Characteristics

Material Code	Relative xr* @ 5Ghz	TCC† Loss ppm/°C	Coefficient of Tangent* % Max	Thermal Expansion ppm/°K	Conductivity W/m-°K
QZ	3.82 (@ 1MHz)	Fused Quartz	0.0015 (@ 1MHz) 0.033 (@ 24Ghz)	0.55	1.28
AG	8.85±0.35 (@ 1MHz)	Aluminum Nitride	0.10	4.6	140-180
PI	9.9±0.15 (@ 1MHz)	Alumina 99.6%	0.01	6.5 - 7.5	27
PG	12.5±0.5	P22±30	0.02	7.6	–
AH	20±0.5	P90±20	0.02	9.6	1.56
NA	23±1	N30±15	0.03	10.1	1.56
CF	25±2	0±15	0.15	9.0	1.56
CD	38±1	N20±15	0.04	5.8	1.59
CG	67±3	0±30	0.10	9.0	1.59
NR	152±5	N1500±500	0.06	10.0	2.72

* Unless otherwise specified K dielectric measurement at approximately 5Ghz

† For the temperature range of -55 to 125°C

Performance characteristics of both standard substrates and some of the custom dielectric materials used by Knowles Precision Devices.

Typical Applications for Thin Film

As mentioned, custom thin-film structures can be manufactured to meet the most precise requirements, from simple patterned submounts to highly complex circuits. In general, if you are building a circuit with size, weight, and power (SWaP) concerns, thin film is a good choice because it can reduce complexity and size while maximizing performance. While there are quite a few applications where thin film is a good fit, let's explore two of the main application types where a build-to-print approach with thin-film technology is an excellent option – heatsinks and standoffs and integrated passive devices (IPDs).

Heatsinks and Standoffs

When designing a heatsink or standoff, considering the thermal and electrical properties is extremely important. As the applications these devices are used in are becoming more compact, yet ever more complex, it is difficult for off-the-shelf heatsinks and standoffs to meet the requirements of many electronic component manufacturers. Thus, many manufacturers are looking for suppliers that can work with them to develop a build-to-print option instead.

While the common materials we use for all types of build-to-print applications were mentioned in Table 1 above, for these components specifically we recommend using Aluminum Nitrides (AlNs) because of their excellent thermal properties. AINs are unique because they have both high thermal conductivity and strong electrical resistance, which is unlike most electrically insulative materials that are also thermally

insulative. As a result, AlN allows electrical systems to dissipate heat quickly to maintain maximum efficiency.

At Knowles Precision Devices, we specialize not only in knowing the best materials to use for your specific application, we are also experts in knowing how to make precise electrical connections in these types of sensitive applications with high-density interconnects. For example, instead of using a standard PCB, which likely cannot reliably withstand the high operating temperatures of these devices and does not allow for control of finer features, we take an approach similar to semiconductor companies and use lithography to make these precise connections.

More specifically, looking at one specialized version of a heatsink, the laser diode submount, this component has incredibly high thermal requirements. When arranged in high densities, heat dissipation for laser diodes becomes even more critical, which makes our thin-film technology a good option. In these high-density components, a long wire bond connection will make the bond worse electrically. Therefore, we use Alumina mounting shorts to create short bonds. This approach allows for placement of a wire bond anywhere in the circuit and replaces the need for gold (Au) terminations on the substrate (Figure 1).

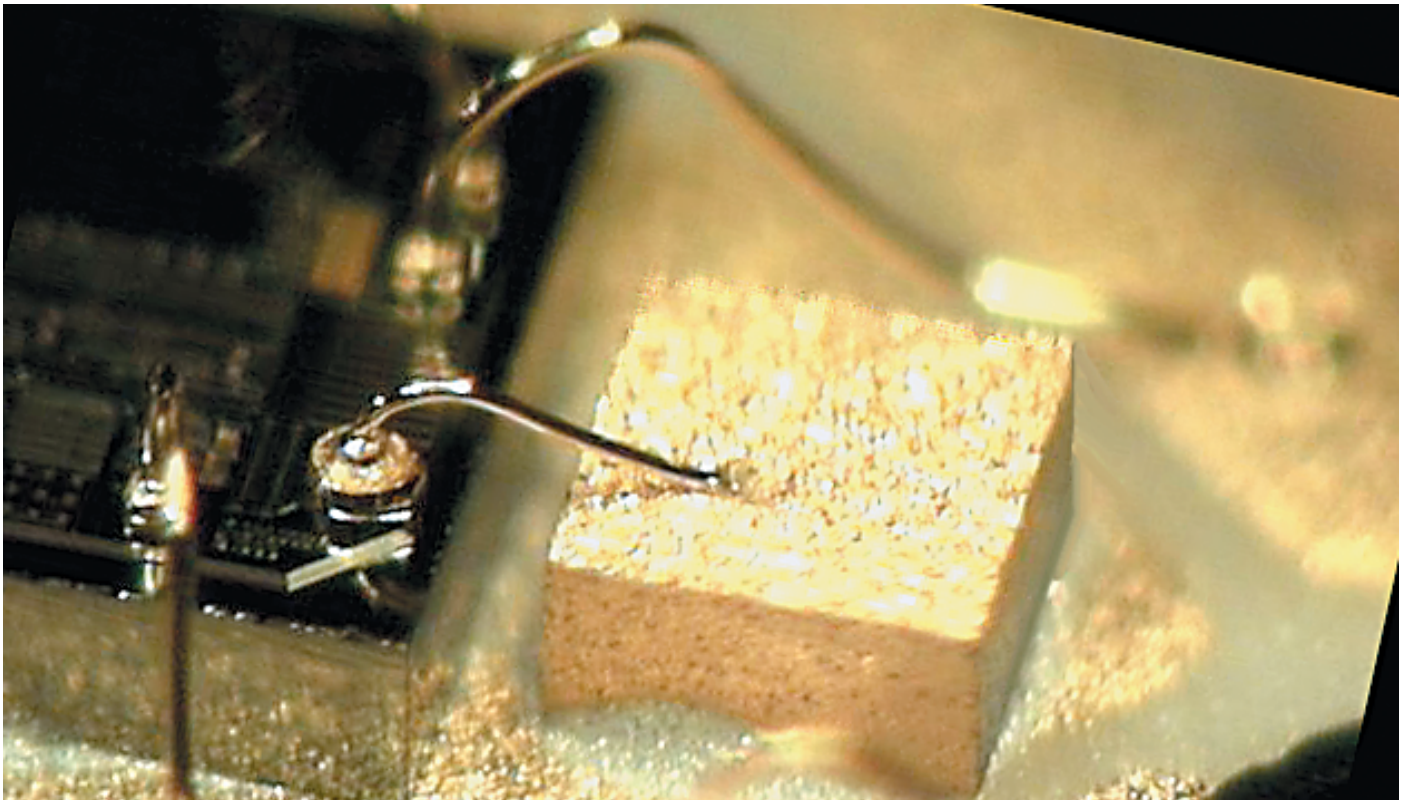


Figure 1 An example of a mounting short used to create a short bond on a laser diode submount.

Integrated Passive Devices

IPDs have been around in some form since the 1960s as a way to reduce the total number of assembly steps in manufacturing a circuit. This approach has gained popularity over the years since it reduces overall manufacturing costs and addresses various SWaP concerns. Ranging from simple to complex, IPDs can combine a variety of circuit building blocks such as conductors, resistors, plated vias, selective high-conductivity traces, integrated resistors, filled vias, bridges, and transmission line structures, into one

device. However, if not done correctly, condensing multiple passive components into a small device can lead to a number of issues.

This is why a build-to-print approach is a great strategy for developing an IPD. Not to pick on the poor old PCB again, but PCBs take up a ton of space relatively. Instead, you can build an IPD with thin film to safely place several connections close together. With this approach, in the end device there is just one component being placed instead of dozens of capacitors and resistors, which is a huge space and time saver. Typical use cases for IPDs include the following:

- Custom resistor capacitor networks – If you can draw it on a napkin, we can make it
- Lange couplers and power combiners
- EMI filters
- High-frequency filters
- Microwave integrated circuits
- Bias decoupling and filtering
- Lumped element impedance matching networks
- PA stabilizations
- Impedance matching and power combining networks

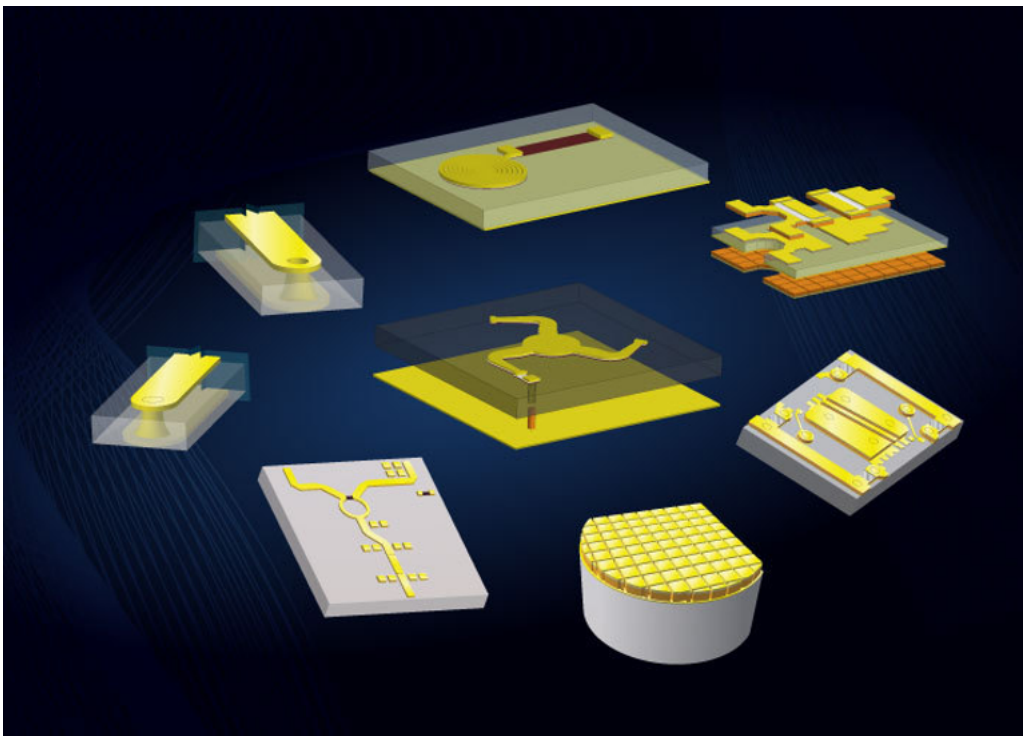


Figure 2 A sampling of IPDs, including a spiral inductor, interposer, and a power divider that we can make.

If You Can Draw It, We Can Make it

From a single capacitor and resistor to a super complex IPD, if you can draw it, and it's within our menu of capabilities, our build-to-print team can make it. Additionally, since we specialize in working with military and aerospace organizations, we are incredibly familiar with making components that are compact and reliable, even in incredibly harsh environments.

Our Build-to-Print Process

This next section provides an overview of some of the main parts of our build-to-print process. These are the main topics our applications engineers review with clients to kick-off any build-to-print project. We will expand on each of these topics throughout the eBook.

Substrate Material

First and foremost, we need to determine the most appropriate substrate material for an application. We stock the most common materials including Alumina, AlN, high-dielectric Titanates, Quartz, and Sapphire, and also have a wide-variety of custom ceramics. We can work with materials of a standard thicknesses from 10 to 40 mil in increments of 5 mil and offer surface finishes of "as fired," lapped, or polished.

Plated Thru Holes and Filled Vias

Next, we need to have a conversation about the size, location, and material required for any plated thru holes or filled vias needed. Our manufacturing facility has multiple CO2 lasers to precisely control the drilling process for thru-holes and vias. Additionally, our Cu-filled vias have been space- and flight qualified by multiple customers and are widely used to achieve cost-effective, high-volume designs at a fraction of the cost of Au-filled vias (Figure 3).

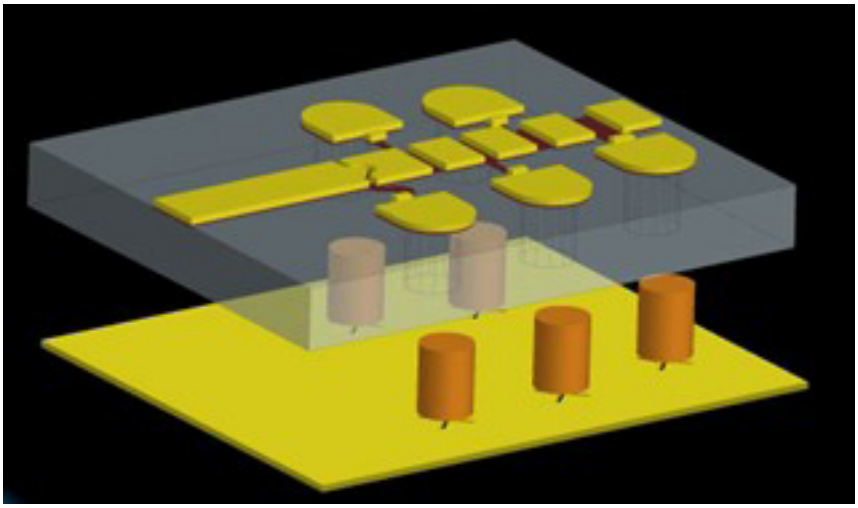


Figure 3 This drawing shows space-qualified Cu-filled vias.

However, for customers requiring Au-filled vias for legacy programs or specific design demands, we also maintain an internal Au-filled via process as well. Of course, we also provide plated thru holes where via fill is not desired or required.

Sputtering

We maintain several multi-target sputter machines with commonly used metals for quick-turn standard delivery without a premium. Adhesion metals consist of titanium (Ti) and titanium tungsten (TiW) as well as chromium (Cr), nickel chromium (NiCr), and tantalum nitride (TaN). Resistors using TaN and NiCr are standard. Barrier metals consist of Ni, Palladium (Pd), and Platinum (Pt), as well as Cr and TiW. Conductors using Cu, Au, and Al are all standard. High-power conductors using Cu or Au are also available. Table 2 below shows proven metallization schemes that we recommend and will elaborate on more later in this eBook:

Table 2 Metallization Schemes

S1	300 Å TiW, 50 µin NiV, 100 µin Au
S2	300 Å TiW, 50 µin NiV, 300 µin AuSn
S5	300 Å TiW, 100 µin Au
S5A	300 Å TiW, 200 µin Au
S7	300 Å TiW, 6 µin Pt, 100 µin Au
S10	300 Å TiW, 100 µin Au, 50 µin Ni / 3-6 µin Au
S10A	300 Å TiW, 200 µin Au, 50 µin Ni / 3-6 µin Au
S12	300 Å TiW, 100 µin Cu, 50 µin Ni / 3-6 µin Au
S12A	300 Å TiW, 200 µin Cu, 50 µin Ni / 3-6 µin Au
S19	50 Ω/ sq. TaN, 300 Å TiW, 100 µin Au

Proven metallization schemes we regularly use in our build-to-print configurations.

Photolithography

Today, some RF circuit designs are approaching the need for the same demanding standards used in the semiconductor industry. Therefore, we have advanced our process to include multiple aligners and use a variety of tooling to manufacture designs to exacting standards. Using a combination of Mylar and glass tooling, we can manage the cost of non-recurring engineering while still providing features as small as 0.0004" (10 um) to tolerances of ±0.0001". We also use selective plating to achieve wire bond or solderability in the standard schemes described above.

Electroplating

For applications where photolithography is not needed, we offer environmentally friendly electroplating capabilities. We offer two different processes depending on client needs – one that is an etch back process and one that uses a sputter seed layer, etch artwork, and then a build-up plating process for the remaining layers.

Dicing

For customers that require high-volume production, we have ever-growing dicing capabilities to provide high-volume throughput of parts as small as .015" x .015" up to a thickness as large as 90 mil. Since dicing is typically a bottleneck in many operations, we strategically expanded this part of our manufacturing process to ensure throughput matches the balance of the operation.

Laser Trim

For applications where resistors have tighter tolerances below our standard bake-in tolerance of ±10 percent, we have resistor trimming available. This could include high-volume throughput for chip resistors, attenuators, and complex circuits. Plunge cut, scan cut, microwave scan cut, ladder networks, and "copy trim" are all aspects of laser trim that can be incorporated into a design for tolerances as small as 1 percent. Additionally, laser cutting is available for areas within the part that need to be removed such as location pins or hard-to-fit parts with profiles that are not geometrically square.

Packaging

Finally, all devices need to be packaged when they are completed. We have comprehensive packaging options readily available including all types of waffle pack, bulk packaging options, and tape and reel services.

To help customers systematically process the decisions required for build-to-print applications and select the right material properties for their applications, we've developed the following simplified process detailed in Figure 4.

Part Number Identification

S	20	CG	250	D	Z	N	X
Product S = Internal H = External	Case Size 10 15 20 25 30 40	Material See Material Table Above	Thickness 100 = 0.010" 155 = 0.0155" 250 = 0.025	Thickness Tolerance D = ± 0.0005 E = ± 0.001	Surface Finish X Y Z S	Metallization See Metallization Table Below	Test Level X K D

Thickness Code A three digit code representing the thickness in mills.
Examples: Code 100 = 0.010", Code 155 = 0.0155", Code 250 = 0.025"
Please consult with an applications engineer for thickness <0.010"

Thickness Tolerance Codes
D = ±0.005 - Machined or Polished
E = ±.001 - Standard

Metallization

Code	Description
X	No Metallization
M	300 Angstroms TiW, 100 µ in. min. Au
N	300 Angstroms TiW, 50 µ in. min. NiV, 100 µ in. min. Au
P	75 µ in. min. Nickel, 100 µ in. min. Au
L	Top 50 Ohms/sq. TaN, 300 Angstroms TiW, 100 µ in. min. Au
	Bottom Side 300 Angstroms TiW, 100 µ in. min. Au
E	Metallized and etched per Customer drawing
T	300 Angstroms min. TiW, 50 µ in. min. NiV, 300 µ in. min. Au-Sn
D	SPECIAL, Customer Drawing Required!

Figure 4 This is graphical representation of the process we use to work with customers to determine the most appropriate material choice for their build-to-print application.

Let's look more closely at some of these decisions and other considerations to discuss with your design team when working on build-to-print applications.

Substrate Selection

All circuit designs begin with the proper choice of substrate. To determine the right fit for your build-to-print application, the following characteristics of the substrate material and your application need to be considered:

- Operating frequency
- Size
- Dielectric constant
- Material type
- Thickness
- Transmission line impedance
- Mechanical requirements (TC, CTE)

Let's start by analyzing the use cases and typical attributes of the five most common substrates used today in Table 3. You can also learn more details on the material properties of each of these substrates here.

Table 3 Substrate Uses and Qualities

Material	Typical Uses	Comments
Alumina (Al203) 99.6%	Low-to-medium power DC/RF microwave circuits using silicon or GaAs ICs standards.	Cost-effective material with a wide range of applications.
Aluminum nitride (AlN)	High-power DC/RF/ microwave circuits using silicon or GaAs ICs standards.	Optimal CTE match with silicon devices
Quartz (Si02)	Microwave/mmWave circuits requiring extremely low loss or low CTE.	Low loss tangent and CTE and a smooth surface finish.
Titanates	RF/microwave amplifiers or oscillators requiring High-Q resonators and transformers.	Dielectric constants available from 12 to 100.
Sapphire	mmWave/optical circuits with special electrical or mechanical requirements.	Low loss tangent and optical surface finish.

This table provides a high-level overview of common use cases and notable qualities for common substrates.

When it comes to these commonly used substrates, we can work with materials of a standard thicknesses from 10 to 40 mil in increments of 5 mil and offer surface finishes of "as fired," lapped, or polished.

Using Knowles Precision Devices' Custom Ceramics on Thin-Film to Significantly Reduce SWaP

In general, if you are building a circuit with SWaP concerns, thin film is a good choice because it can reduce complexity and size while maximizing performance. Therefore, in addition to our extensive experience working with the five common materials noted above, we also produce a variety of high-K substrates that are ideal for circuit miniaturization using our thin-film process as these materials offer the following benefits:

- Size reduction – Smaller and lighter systems
- Thin-film precision – Excellent repeatability and no tuning
- Improved field confinement
- Improved temperature stability
- Lower CTE mismatch stress in surface mount applications
- Reduced costs

More specifically, we offer a variety of high K substrates that are ideal for circuit miniaturization using our thin-film process. Table 4 shows the properties of some of our custom high K materials alongside some of the most common standard materials.

Table 4 High K Material Properties

Material Code	Relative xr* @ 5Ghz	TCC† Loss ppm/°C	Coefficient of Tangent* % Max	Thermal Thermal Expansion ppm/°K	Conductivity W/m-°K
QZ	3.82 (@ 1MHz)	Fused Quartz	0.0015 (@ 1MHz) 0.033 (@ 24Ghz)	0.55	1.28
AG	8.85±0.35 (@ 1MHz)	Aluminum Nitride	0.10	4.6	140-180
PI	9.9±0.15 (@ 1MHz)	Alumina 99.6%	0.01	6.5 - 7.5	27
PG	12.5±0.5	P22±30	0.02	7.6	–
AH	20±0.5	P90±20	0.02	9.6	1.56
NA	23±1	N30±15	0.03	10.1	1.56
CF	25±2	0±15	0.15	9.0	1.56
CD	38±1	N20±15	0.04	5.8	1.59
CG	67±3	0±30	0.10	9.0	1.59
NR	152±5	N1500±500	0.06	10.0	2.72

* Unless otherwise specified K dielectric measurement at approximately 5Ghz
† For the temperature range of -55 to 125°C

This table provides an overview of the material properties for some of our most popular high K materials.

Metallization

Once the appropriate substrate is identified, the next critical parameter to evaluate is the selection of metallization. This includes making decisions on a variety of factors such as solderability, solder types, solder hierarchy, circuit attach, skin depth, conductivity, and thermal extremes. Typically, depending on what is decided, metallization ends up being the single largest factor in determining lead time and compatibility of processes.

Standard Metallization Systems

Standard metallization systems consist of materials for four different layers – resistor, adhesion, barrier, and conductor. Some of the common material schemes we recommend for the adhesion, barrier, and conductor layers include the following:

- TiW/Au, TiW/Ni/Au, TiW/Pd/Au and TiW/Cu/Ni/Au with TiW forming the main adhesion layer
- Ni or Pd (optional) functioning as a barrier layer for solderable devices
- Au or Cu as the main conductor, where Au can be fully sputtered or plated to various values of thickness to enhance skin depth and conductivity (discussed more below)

When it comes to the resistor layer, this layer is deposited before adhesion layers due to post processing requirements. TaN is the most common resistor material used because it offers well-established self-

passivating characteristics. For applications where minimum resistor change over temperature extremes is critical, NiCr resistor films are a good choice. Various sheet resistance values are available depending on the resistor range for the overall design. More details on the typical values of various materials and characteristics of common combinations we use are included in Table 5 and Table 6 below.

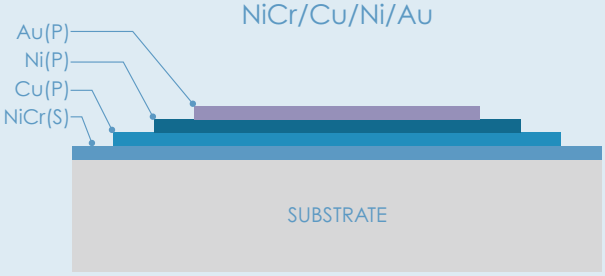
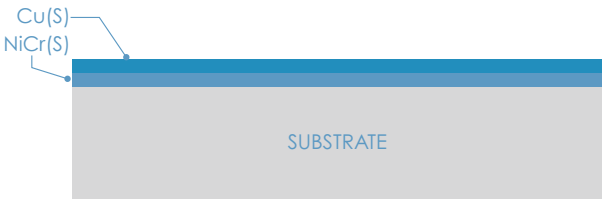
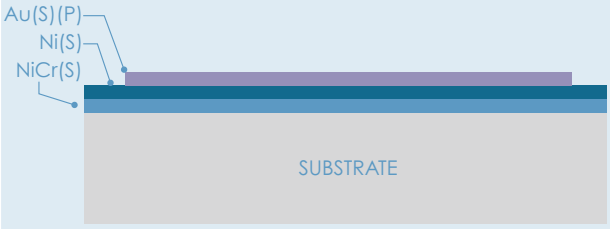
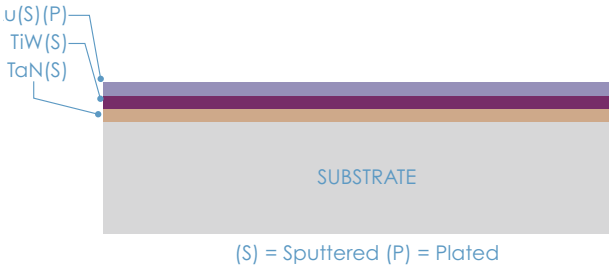
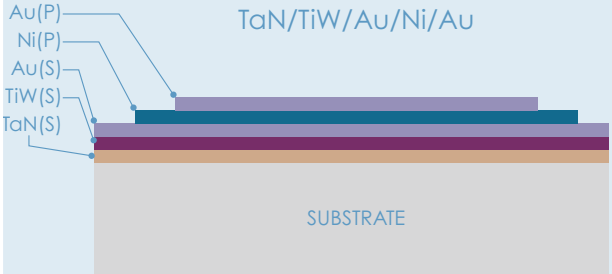
Table 5 Materials and Values for Each Layer

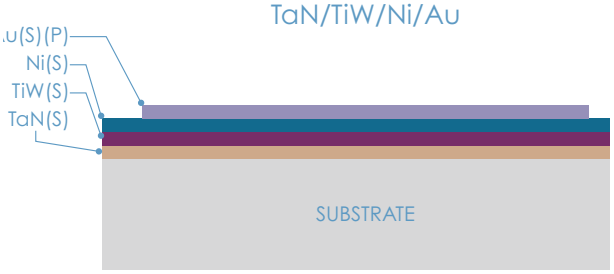
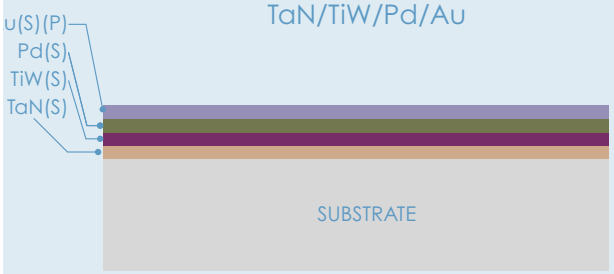
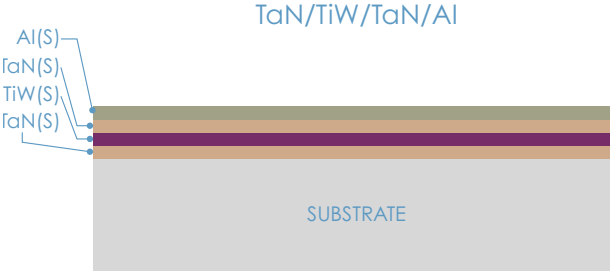
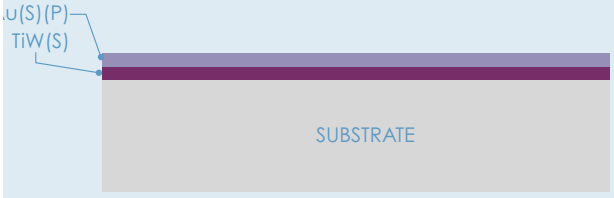
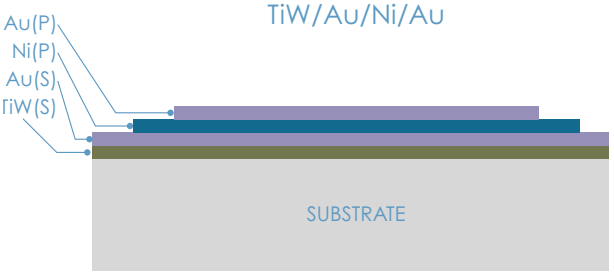
Function	Materials	Typical Values
Resistor	TaN, Tantalum Nitride	8–150 ohms/square[1]
	NiCr, Nickel Chromium Alloy	25–300 ohms/square[1]
Adhesion	TaN, Tantalum Nitride	250–1000 Angstroms
	NiCr, Nickel Chromium Alloy	250–1000 Angstroms
	Cr, Chromium[4]	250–750 Angstroms
	Ti, Titanium	500–1000 Angstroms
	TiW, Titanium Tungsten Alloy	250–750 Angstroms
Barrier	Cr, Chromium[4]	250–750 Angstroms
	TiW, Titanium Tungsten Alloy	250–750 Angstroms
	Ni, Nickel (sputtered)[2 4]	1000–2000 Angstroms
	Ni, Nickel (plated)[4]	50–300 microinches
	Pd, Palladium[3 4]	1000–2000 Angstroms
Conductor	Aluminum (sputtered)	50–200 microinches
	Copper	20–200 microinches
	Gold	20–200 microinches
High Power Conductors	Copper/Nickel/Au[3 4]	500–3000 microinches
	Gold[3]	400–800 microinches

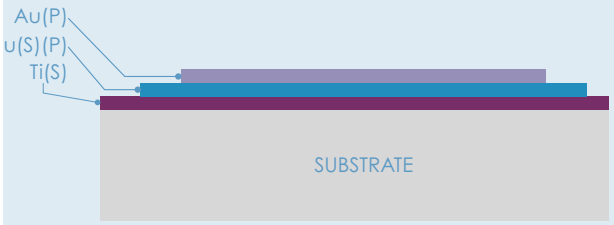
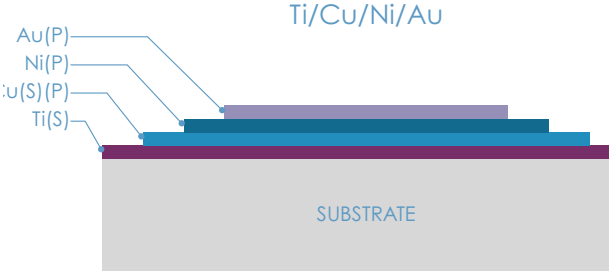
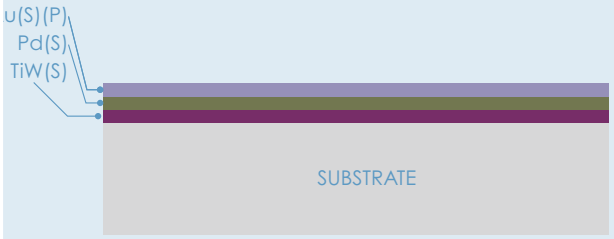
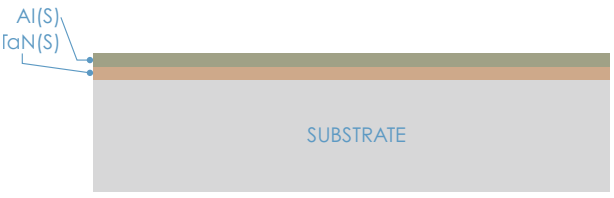
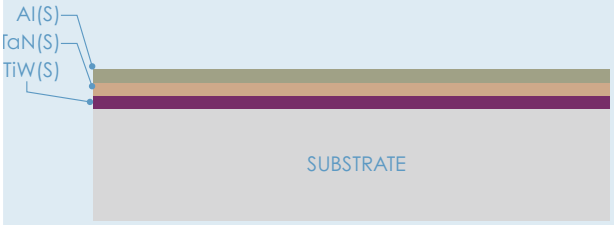
1 - Post heat treatment
2 - Pure Nickel
3 - Limited minimum feature size
4 - Temperature limited due to metal diffusion

This table shows the typical functions and values for various materials commonly used for each layer.

Table 6 Common Metallization Schemes

Metal System (Drawings not to scale)	Bondable		Fine Lines	High	Solderable		
	Au/ Wire	Al/ Wire	< .002"	Power	Pb Bearing	RoHS	Au Bearing
NiCr/Cu/Ni/Au  (S) = Sputtered (P) = Plated	Y	N	N	Y	Y		Y
NiCr/Cu  (S) = Sputtered (P) = Plated	N	N	N	Y	Y		N
NiCr/Ni/Au  (S) = Sputtered (P) = Plated	Y	N	Y	Y	Y		Y
TaN/TiW/Au  (S) = Sputtered (P) = Plated	Y	N	Y	N	N		Y
TaN/TiW/Au/Ni/Au  (S) = Sputtered (P) = Plated	Y	N	Y	Y	Y		Y

Metal System (Drawings not to scale)	Bondable		Fine Lines	High	Solderable		
	Au/ Wire	Al/ Wire	< .002"	Power	Pb Bearing	RoHS	Au Bearing
TaN/TiW/Ni/Au  (S) = Sputtered (P) = Plated	Y	N	Y	Y	Y		Y
TaN/TiW/Pd/Au  (S) = Sputtered (P) = Plated	Y	N	N	N	Y		Y
TaN/TiW/TaN/Al  (S) = Sputtered (P) = Plated	N	Y	N	N	N		N
TiW/Au  (S) = Sputtered (P) = Plated	Y	N	Y	N	N		Y
TiW/Au/Ni/Au  (S) = Sputtered (P) = Plated	Y	N	Y	Y	Y		Y

Metal System (Drawings not to scale)	Bondable		Fine Lines	High	Solderable		
	Au/ Wire	Al/ Wire	< .002"	Power	Pb Bearing	RoHS	Au Bearing
Ti/Cu/Au	Y	N	N	Y	Y		N
 (S) = Sputtered (P) = Plated							
Ti/Cu/Ni/Au	Y	N	N	Y	Y		Y
 (S) = Sputtered (P) = Plated							
TiW/Pd/Au	Y	N	N	N	Y		Y
 (S) = Sputtered (P) = Plated							
TaN/Al	N	Y	N	Y	N		N
 (S) = Sputtered (P) = Plated							
TiW/TaN/Al	N	Y	N	N	N		N
 (S) = Sputtered (P) = Plated							

This table includes diagrams and additional functional details for common metallization systems we recommend for our build-to-print customers.

Adhesion Layer Thickness

To support the metallization schemes in Table 6, we recommend best practices on adhesion layer thickness based on the design provided for review. To achieve the best possible metal adhesion for your design, consider the following recommendations for adhesion layer thicknesses for TiW for your design:

- 500 ± 250 Å (simple patterns/conductor only)
- 1,000 ± 250 Å (for plated thru vias and slots)
- 1,250 ± 250 Å (for filled vias)

If your design is different than the standard process considerations listed above or has special characteristics such as vias and edge castellations, we also can make custom recommendations that best suit your application needs.

Platting vs. Sputtering for Thicker Metals

Some designs need thicker conductors for skin depth requirements or to meet incorporated company standards. The common technique of sputtering can have several negative impacts at increased thicknesses. First, it is costly to deposit precious metals and then etch the circuit features. Second, thick sputtered structures that are subsequently chemically etched undercut the patterned resist due to the isotropic nature of the process. This results in a cross-sectional profile that is more trapezoidal than square.

Instead, structures thicker than 100µ" benefit from using a selective plating technique to create the circuit. This method eliminates the negative attributes of an etch-back process. Therefore, for applications where thicker materials and sidewall control is critical, we offer in-house plating capabilities.

Conductor Dimensions for Standard and Multilayer Conductors

All circuit designs contain critical dimensions necessary for compliance and performance. It is important to consider these dimensions when designing the circuit to avoid adding unnecessary costs to the design. It is also important to note that conductor tolerances of <0.001" require more costly tooling to ensure compliance. We will touch on this topic more in the conductors section of this eBook.

While many organizations use the same metallization on every product because "that's how it's always been done," as part of our build-to-print process, we believe that it is best to consult with the sales engineer or factory regarding the options available to meet your specific requirements. This extra discussion will always result in the optimum metallization for your specific application.

Laser Techniques

At this point in the build-to-print process, you've already determined the best substrate material and metallization scheme for your application. Now it's time to establish the best processes to use to make everything all physically fit together and function appropriately. The following laser cutting techniques, from least to most precise, may be required for your project:

- **Laser scribing –** The ceramic substrate is perforated by the laser so the customer can break apart the ceramic at the appropriate point when ready to use.
- **Laser machining –** Used to cut the ceramic materials to make the "puzzle pieces" that form each plate.
- **Laser trimming –** A high-precision technique where lasers are used to carefully remove small bits of resistive metallization on the ceramic to make final adjustments to bring the part into spec. This includes techniques such as plunge, scan, and serpentine cuts.
- **Laser obliteration –** This is similar to laser trimming but can remove Au, Ni, and Cu to achieve high-precision tolerances.

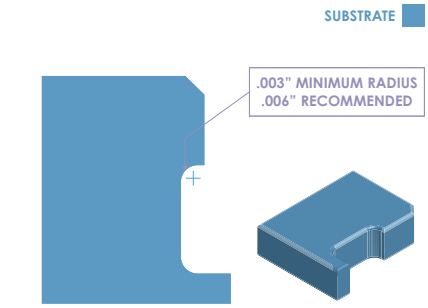
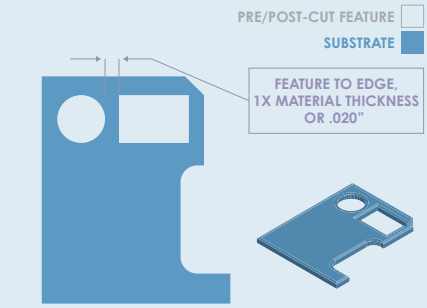
Before jumping into more details on these techniques, let's first look at the different lasers that can be used for these processes. In general with lasers, the smaller the wavelength, the more capable it is of performing high-precision cuts. Therefore, the following three types of lasers can be used to perform different jobs – CO^2, fiber, and UV lasers.

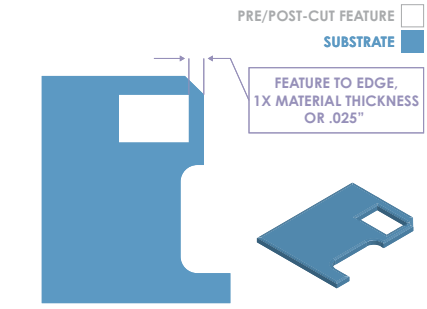
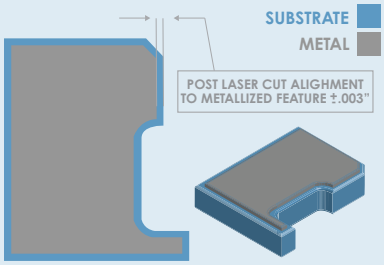
Starting with the CO^2 laser, invented in 1964, this is one of the oldest types of gas lasers. Because it offers high power and is relatively low cost, it is a common laser machining workhorse. Similarly, fiber lasers use doped fiber as the gain medium. These lasers are also high power and can offer a range of wavelengths, and therefore different precision compared to the CO^2 lasers. And finally, UV Lasers, as the name implies, operate at much smaller wavelengths compared to CO^2 and fiber lasers. This means UV lasers offer much tighter control over feature size, making them ideal for very precise and tiny cuts, like those needed for laser trimming and obliteration.

A Closer Look at the Various Laser Techniques

As mentioned, laser machining is the process used to make initial cuts to the substrates used to make thin-film devices. We recommend following the guidelines outlined in Table 7 for laser machining.

Table 7 Guidelines for Laser Machining Techniques

Property	Value and Tolerances	Comments
Maximum Thickness	.060"	Thicker materials require factory consultation
MINIMUM RADIUS 	.003"	CO^2 beam width = .003", use .006" min. radius to change cut direction
Smallest Feature	0.6:1(ratio) minimum diameter	
to material thickness		
Front-to-Back Taper	10 – 15 percent of material thickness	Includes bell effect at entrance
Via Hole for Plated Thru Connection	0.8:1 (ratio) hole diameter to material thickness	Measured at exit, account for metal annulus on circuit side
Via Hole Filled	0.7:1 (ratio) hole diameter to material thickness	Account for metal annulus on circuit side
Feature Size Tolerance	± .002"	Non-cumulative
PRE/POST-CUT FEATURE TO FEATURE 	1X material thickness	Not less than .020"

Property	Value and Tolerances	Comments
PRE/POST-CUT FEATURE TO EDGE 	1X material thickness	Not less than .020"
POST LASER CUT ALIGNNMENT TO METALLIZED FEATURES 	± .003"	All cutouts require a .003" pullback of backside metal
Diamond Sawing	± .001" min	± .002" Standard

These are our recommended guidelines for holes machined features using laser machining techniques.

When working on your thin-film design, it's a good idea to discuss requirements such as feature spacing, minimum radius, and via taper with your applications engineer. Additionally, our engineers can perform some unique laser machining processing that you should be sure to discuss with your applications engineer as well.

Similarly, Table 8 shows the laser scribe specs we recommend following.

Table 8 Laser Scribing Guidelines

Nominal Substrate Thickness		Rsultant Segment Tolerance From Two Broken Edges		Laser Scribed Edge of Board to First Scribe Line	
English	Metric	English	Metric	English	Metric
0.010"	0.254 mm	+0.006" -0.002"	+0.15 mm -0.05 mm	+0.004" -0.002"	+0.10 mm -0.05 mm
0.015"	0.381 mm	+0.006" -0.002"	+0.15 mm -0.05 mm	+0.004" -0.002"	+0.10 mm -0.05 mm
0.020"	0.508 mm	+0.006" -0.002"	+0.15 mm -0.05 mm	+0.005" -0.002"	+0.13 mm -0.05 mm
0.025"	0.635 mm	+0.006" -0.002"	+0.15 mm -0.05 mm	+0.005" -0.002"	+0.13 mm -0.05 mm
0.030"	0.762 mm	+0.008" -0.002 "	+0.020 mm -0.05 mm	+0.006" -0.002"	+0.18 mm -0.05 mm
0.035"	0.889 mm	+0.008" -0.002 "	+0.020 mm -0.05 mm	+0.007" -0.002"	+0.18 mm -0.05 mm
0.040"	1.02 mm	+0.008" -0.002 "	+0.020 mm -0.05 mm	+0.007" -0.002"	+0.18 mm -0.05 mm
0.050"	1.27 mm	+0.008" -0.002 "	+0.020 mm -0.05 mm	+0.007" -0.002"	+0.18 mm -0.05 mm
0.060"	1.52 mm	+0.014" -0.002"	+0.36 mm -0.05 mm	+0.010" -0.002"	+0.25 mm -0.02 mm
0.080"	2.03 mm	+0.020" -0.004"	+0.51 mm -0.10 mm	+0.012" -0.003"	+0.30 mm -0.08 mm
0.100"	2.54 mm	+0.025" -0.004"	+0.64 mm -0.10 mm	+0.14" -0.003"	+0.36 mm -0.08 mm
0.120"	3.05 mm	+0.025" -0.004"	+0.64 mm -0.10 mm	+0.14" -0.003"	+0.36 mm -0.08 mm

These are our recommended guidelines for laser scribing.

For applications where resistors have tighter tolerances below our standard bake-in tolerance of ±10 percent, we have resistor trimming available. This could include high-volume throughput for chip resistors, attenuators, and complex circuits. Plunge cut, scan cut, microwave scan cut, ladder networks, and "copy trim" are all aspects of laser trimming that can be incorporated into a design for tolerances as small as 1 percent. Additionally, laser cutting is available for areas within the part that need to be removed such as location pins or hard-to-fit parts with profiles that are not geometrically square.

Knowles Precision Devices Has In-House Laser Expertise

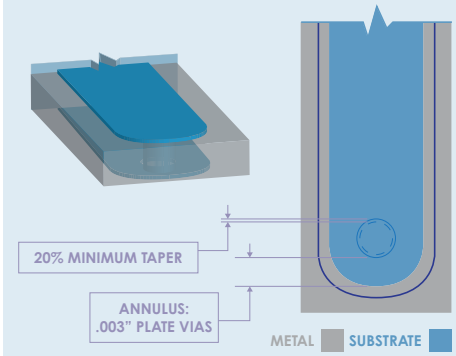
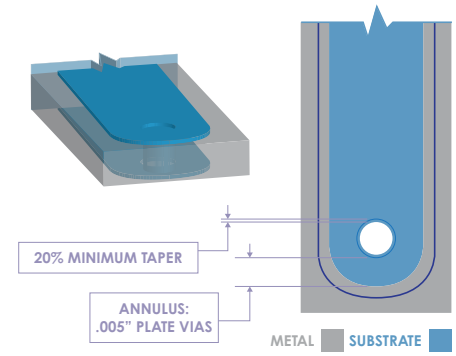
We understand that lasers do not operate uniformly across materials. It takes a lot of know-how and craftsmanship to drive these lasers to precisely machine thin-film components. Not only do operators need to know how to use the lasers, which takes a unique skill set in itself, they also need to have an in-depth understanding of how the laser beams will interact with the different materials.

This is why we don't outsource this work. We have the expertise to perform all the above-mentioned techniques with the appropriate lasers in-house in our extremely precise machine shop. Our precision machinists know how to get things just right on the wide variety of materials we work with. These are critical skills for building components with tight tolerances and hard-to-fit parts with profiles that are not geometrically square.

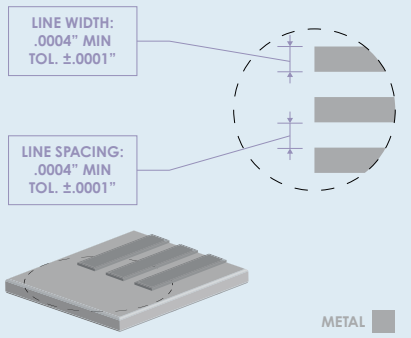
Conductors

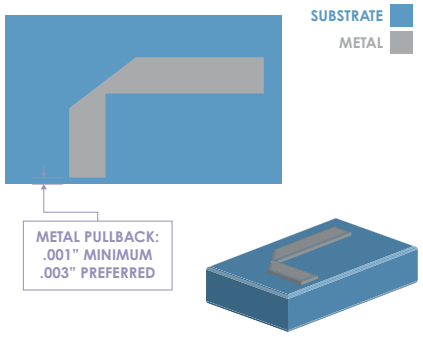
In our overview of metallization we touched on the conductor layer as one of the four layers in a standard metallization system. Now it's time to take a more in-depth look at this layer. In general, the conductor layer for all circuit designs contains critical dimensions necessary for compliance and performance. It is important to consider these dimensions as outlined in Table 9 below when designing thin-film circuits both to achieve appropriate functionality and to not add unnecessary cost to the design.

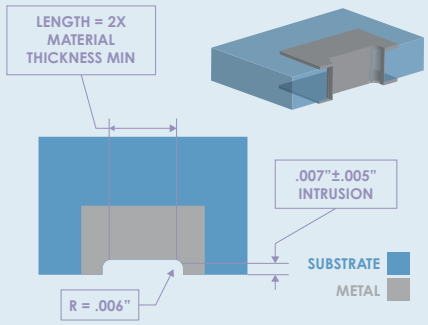
Table 9 Multilayer Conductor Standard Layout Guidelines

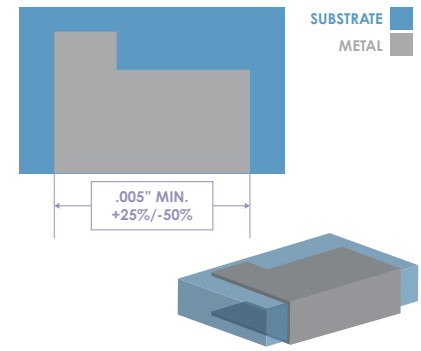
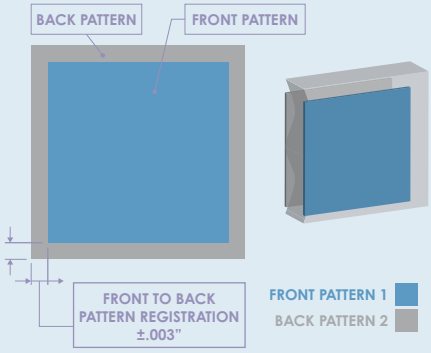
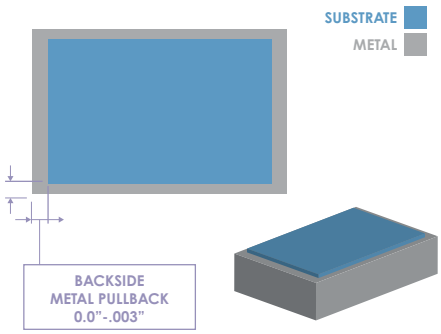
Feature	Values and Tolerances	Comments
FILLED VIAS 	.003"	Per side 20 percent minimum taper
PLATE VIAS 	.005"	Per side 20 percent minimum taper

Feature	Values and Tolerances	Comments
LINE & SPACING WIDTH	.0004 minimum ± .0001"	Minimum space widths and minimum line widths are a function of conductor thickness
METAL PULLBACK	.001" minimum	.003" preferred
RADIAL EDGE WRAP	.007" ± .005"	.006" typical radius, length 2x material thickness

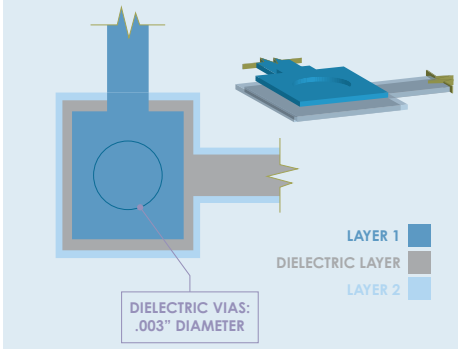
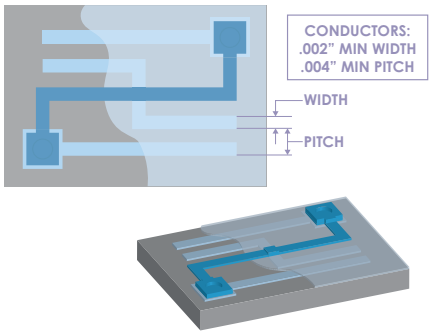
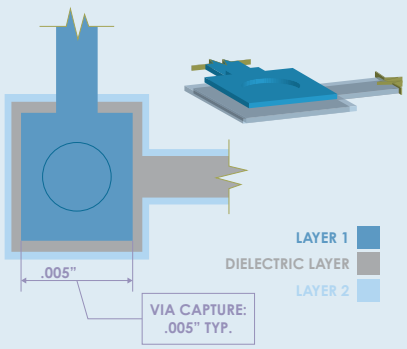






Feature	Values and Tolerances	Comments
	.005" minimum +25%/-50%	Increase or decrease of design area
STRAIGHT EDGE WRAP		
		
	± .003"	± .001" by request
FRONT TO BACK PATTERN REGISTRATION		
		
	0 - .003"	
BACKSIDE METAL PULLBACK		
		

*Conductor tolerances of <0.001" will require more costly tooling to ensure compliance.

Feature	Values and Tolerances	Comments
DIELECTRIC VIA DIAMETER 	.003" Diameter	Ground signal ground up to 2 levels
CONDUCTORS WIDTH 	.002" width .004" pitch	Ground signal ground up to 2 levels
VIA CAPTURE 	.005"	

This table shows the guidelines for standard layouts for basic and multilayer conductors.

Fine Line Conductor Features

Devices such as filters, diplexers, Lange couplers, directional couplers, interdigitated capacitors, and spiral inductors rely on the precision of conductor line width and line spacing to achieve targeted performance. As a result, there are a number of features that will vary depending on the line widths used in the conductor layer with various materials (Table 10).

Table 10 Minimum Line Width Characteristics by Metal Type

Metal Layer	With Vias - Minimum Line Width/Spacing	Without Vias - Minimum Line Width/Spacing
Au (10 to 150 µ") (sputtered)	1.0	0.8
Au (150 to 300 µ") (sputtered)	1.5	1.0
Au (300 to 800 µ") (sputtered)	3.0	3.0
Cu (50 to 600 µ") (sputtered)	3.0	3.0
Cu (0.5 to 6 mils) (plated)	3.0	3.0
NiV (50 to 125 µ") (sputtered)	3.0	3.0

Minimum line width and conductor spacing tolerance for Au, Cu, and NiV conductors.

First, the characteristic impedance of transmission lines is governed by line widths. Next, the coupling between transmission lines and the control of the even and odd mode impedance to implement couplers and filters is governed by the line widths and the spacing between the adjacent transmission lines.

Additionally, the precise control of the spacing between the coupled lines ensures uniformity in voltage standing wave radio (VSWR) and coupling necessary to make coupler and filter performance repeatable. Edge acuity is also dependent on the thickness of the metal layers required, but generally is less than 0.1 mil. By selecting the proper substrate/metallization system, excellent edge acuity can be achieved, and finished line widths will be within ±0.1 mils of the design dimension.

Finally, fine line width and line space geometries are impacted by the quality of the ceramic surface. Some materials used in thin-film products have grain structures and surface imperfections that may cause the loss of control of fine line widths and line space geometries. While polishing can be used to improve the quality of the surface, this technique is also somewhat limited since some materials do not hold up well to the forces created during polishing. However, one material that is not as limited is polished alumina. The surface quality is high and 1 mil line width/spacing is possible and repeatable when vias are present while 0.75 mil line width/spacing is possible and repeatable when vias are not used.

Vias

A via is a small opening in a circuit that allows for a conductive connection between different layers in the circuit or a connection to the ground-plane. In any circuit medium, vias can offer many advantages. However, we often see many designs that overpopulate ground areas as well as poorly placed vias that can degrade yield due to reduced substrate durability in manufacturing. Therefore, it is critical in hard substrate manufacturing to carefully consider via quantity and location.

Our CAD services can optimize your design by balancing electrical needs with manufacturing enhancements. One of the first determinations we will help you make is if a standard via or a reinforced via – plated or filled – is the best option for your design. Figures 5, 6, and 7 show diagrams of what each via designs looks like and Table 11 provides a high-level overview of the characteristics of plated versus filled vias in an Alumina substrate.

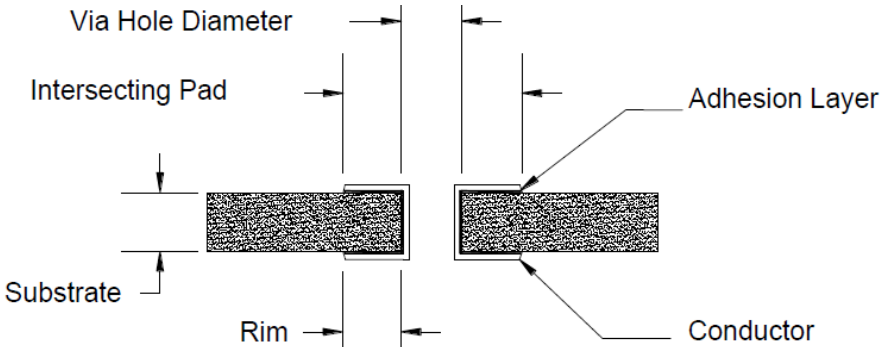


Figure 5 A diagram of a standard via.

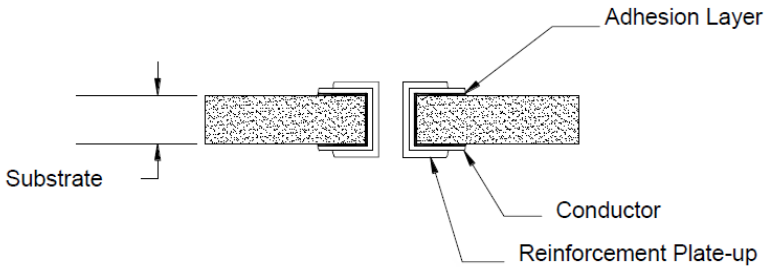


Figure 6 A diagram of a plated via.

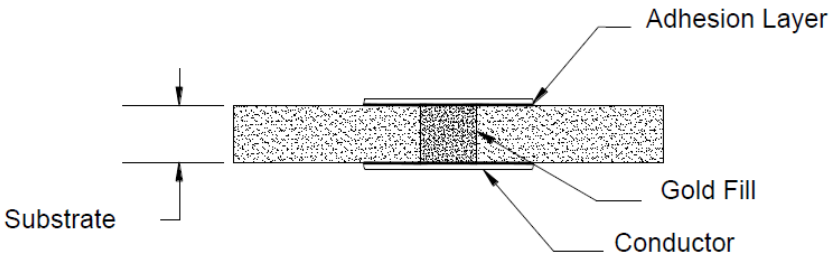
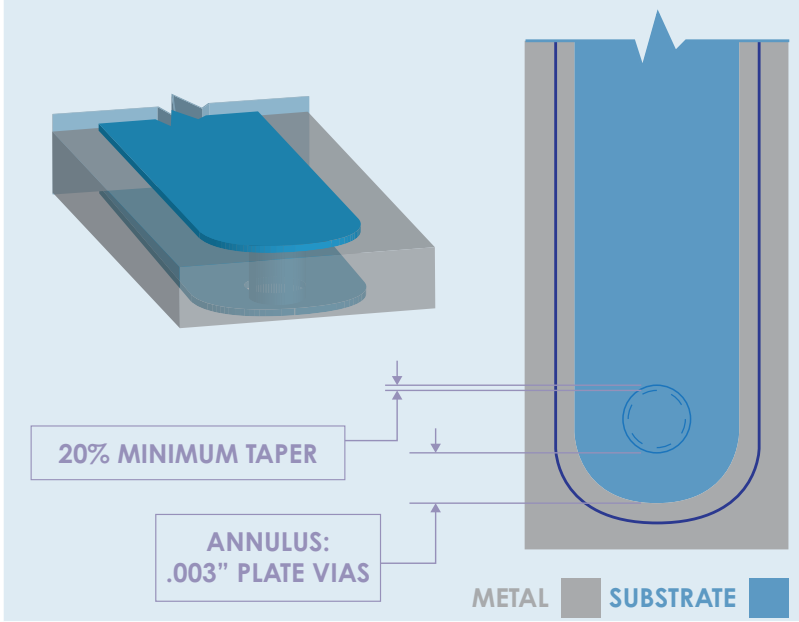
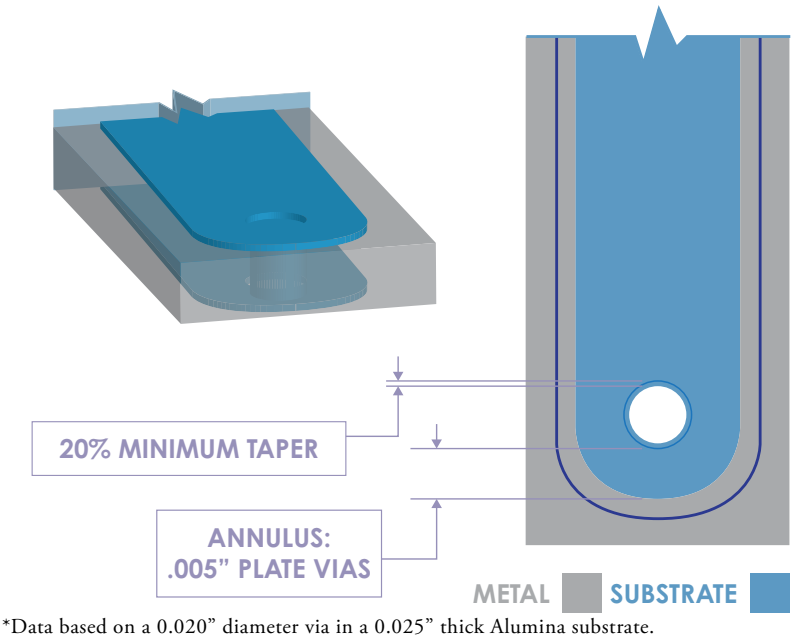


Figure 7 A diagram of a filled via.

Table 11 Comparison of Types of Vias

Feature*	DC Resistance	Inductance	RF Resistance
FILLED VIAS 	1 mΩ	78pH	4 mΩ
PLATE VIAS 	4 mΩ	81pH	14 mΩ

*Data based on a 0.020" diameter via in a 0.025" thick Alumina substrate.

This table provides an overview of the general characteristics of plated vs. filled vias.

Our Approach to Plated Vias

For most applications that need plated vias, standard metal thickness through the holes is acceptable. The preferred and allowable diameters for vias on substrates of varying thicknesses are listed in Table 12 below.

Table 12 Characteristics of Plated Through Vias

Substrate Thickness	Substrate Material	Preferred Via Diameter	Allowable Via Diameter	Via Spacing	
				Center-Center	Center-Edge
.005"	Al2O3	.005"	.003" - .005"	.027"	.023"
.010"	Al2O3,AlN	.010"	.006" - .010"	.030"	.025"
.015"	Al2O3,AlN	.015"	.008" - .015"	.035"	.027"
.020"	Al2O3,AlN	.020"	.010" - .020"	.040"	.030"
.025"	Al2O3,AlN	.025"	.012" - .025"	.045"	.033"
.040"	Al2O3,AlN	.032"	.024" - .040"	.060"	.040"
.050"	Al2O3,AlN	.040" - .050"	.025" - .050"	.070"	.045"

This table highlights the characteristics of plated through vias on various substrate thicknesses.

If higher currents are required, the plated via may need to be reinforced. Reinforcement may also be necessary to reduce RF loss in devices such as interdigital band pass filters. This is done through a separate additional processing plating step where we add additional metal in and around the via to give better mechanical strength and lower via hole resistance. Known as selective plating, this process involves the application of different metal systems in selected areas of a circuit or an additional plate of the same metal in selected areas. This could include the addition of an Ni metal layer in an area where solder is required, or it could involve increasing the metal thickness in via walls without using Ni on the resonators for the filters.

An Overview of Our Approach to Filled Vias

One method of enhancing a design, especially if you need to layer components, is to use filled vias. Filled vias provide a good thermal path and ground return path from the top side conductors to the backside ground plane. We use industry-preferred solid Cu and Au processes as opposed to the less-desirable glass/metal paste method used by other companies. Table 13 provides a general overview of via characteristics on substrates of varying thicknesses and materials.

Table 13 Characteristics of Plated Filled Vias

Substrate Thickness	Substrate Material	Preferred Via Diameter	Allowable Via Diameter	Via Spacing	
				Center-Center	Center-Edge
.010"	Al2O3	.008"	.028"	.020"	Cu,Au
.015"	Al2O3	.012"	.034"	.020"	Cu,Au
.020"	Al2O3,AlN	.016"	.032"	.020"	Cu,Au
.025"	Al2O3,AlN	.020"	.040"	.025"	Cu,Au

This table highlights the characteristics of plated filled vias on various substrate thicknesses.

Additionally, our process using solid Cu-filled vias offers the following advantages versus using solid Au-filled vias:

- Cost effective – 10 to 20 percent cheaper
- Thermal conductivity is 33 percent greater
- Lead time is 20 percent shorter
- Acceptable for prototyping through high-volume production quantities
- Can withstand up to +300°C processing temperatures
- Qualified for use in aerospace applications

In summary, no matter what type of via is needed for your build-to-print design, our team will use the best techniques in the industry to ensure all your requirements are met.

Resistors

As discussed in the metallization section, TaN is the most common resistor material we use. This is because TaN offers higher maximum exposure temperature, a wider annealing window, superior resistance to the harsh environment encountered in soldering and other processing, and well-established self-passivating characteristics. For applications where minimum resistor change over temperature extremes is critical, we believe that NiCr resistor films are a better choice. Table 14 shows the difference in performance for these two types of materials during 1,000-hour test.

Table 14 Resistor Data

Substrate Material	Resistor Film	TCR Range (ppm/°C)	Sheet RHO Ω/sq HTT	Stability
Al2O3, AlN	TaN2	-125±25	25-150	<0.5%
Al2O3	NiCr**	0-25	50-250	<0.5%

**Proprietary Alloy.

Note: All Tests are performed in forced air convection furnaces on untrimmed resistors.

Key Design Parameters for Resistors

When working on a build-to-print design, the key design parameters for resistors that we discuss with customers include resistor value, stability with time and temperature, and power handling. Additionally, the design of a thin-film resistor is governed by the following equation:

$$R = \rho L/Wt$$

Where:

R = Total Resistance (Ω)
ρ = Bulk Resistivity of Resistor Material (Ω-cm)
L = Resistor Length (cm)
W = Resistor Width (cm)
t = Resistor Thickness (cm)

To ease design requirements, a parameter known as sheet resistivity (Rsheet), which is a measure of the resistance of thin films that are nominally uniform in thickness, is also considered. Sheet resistivity assumes L = W in the above equation, making the following equation apply instead:

$$\mathbf{R_{sheet} = RS = \rho/t\ (\Omega/square)}$$

Therefore, simply multiplying RS by L divided by W yields the actual resistance, or

$$\mathbf{R_{Total} = R_{sheet} \times L/W}$$

Additionally, various sheet resistance values are available depending on the resistor range for the overall design.

While sheet resistivity selection should be left to the manufacturer when possible to maximize yield and reduce costs, when sheet resistivities must be specified, the overall range and tolerance requirements need to be balanced to obtain the optimum choice for processing. Some other considerations to note are that resistor tolerances of ±10 percent usually require trimming, although some designs can achieve ±5 percent without it. Resistor tolerances of less than ±2 percent will affect manufacturing yield in terms of the volume, and for resistor tolerances ≤ 1 percent, we recommend contacting our engineers for further design considerations to optimize yield.

Resistor Layer Implementation

The resistor metallization layer for all the resistors on a given circuit is deposited in a single sputter operation. Thus, resistors on a single part must share the same resistivity. We typically use 50 Ω per square for most designs. Table 15 below shows the standard resistor parameters for electrical design as well as allowable limits when using TaN.

Table 15 Standard resistor parameters

Thin-Film Resistors	TaN
Available Sheet Resistivity	25 - 150 Ωsq, 50 - 100 Ωsq preferred
Temperature Coefficient of Resistance (-25°C to 125°C)	-75 to – 100 (ppm/°C)
Stability (Change after 1,000 hours @ 125°C)	.02 percent
Short-Term Exposure Max Temperature (2 minutes)	450°C*

*If Ni is used in the system, drop exposure temperature to 350°C

Standard resistor parameters for electrical design and allowable limits when using TaN

Finally, there are two fundamental resistor layout techniques we use – the notched resistor implementation and the flush resistor process (Figure 8). A general resistor layout guide is also shown in Table 16.

Figure 8 The drawing on the left shows a notched resistor process using an island method while the drawing on the right uses a flush resistor process with an etch-back method.

Table 16 Resistor Layout Guides

Parameter	Limit	Comments
Minimum Tolerance	1 percent (with laser trim)	10 percent standard, 20 percent preferred
Minimum Spacing Between Resistor Selections	.001 inch	Serpentine resistor layouts
Minimum Length and/or Width	.002 inch	Resistor material
Minimum Conductor Pad Size	.003 inch x .003 inch	
Conductor/Resistor Overlap	.0005 inch per side	
Pre-Trim Designed Value	-20 percent	Laser trimmed resistors
Nominal Sheet Resistance	25 – 100 Ωσq	Preferred: 50 Ωsq

The guidelines we recommend following when developing resistors.

Ensuring Reliable Connections with Supported Bridges and Solder Dams

You can have a beautifully designed circuit, but if you can't reliably connect the various components within the circuit, your beautiful design is negated. Let's look at some of the materials and techniques we use for soldering and bridging, and how we handle these techniques as circuit complexity increases.

Soldering Options

As we touched on in the metallization section, the solder layer, and any corresponding necessary solder barriers, are an important part of any circuit design. Previously, solders containing lead were commonly used, but in recent years the elimination of lead from electronic devices as mandated by the Restriction of Hazardous Substances (RoHS) directive is driving a transition among many circuit designers regarding the materials needed for the solder layer. Thus, we offer pre-deposited and patterned Au/Sn solder. On designs with multiple solder hierarchy or multiple pre-form sites, this can be a cost-effective method for eliminating pre-forms.

More specifically, our Au/Sn eutectic is a sputtered material (Au,80.4/ Sn,19.52 - Weight %, Typ); which provides superior flatness and thickness control. Typically, sputtered films can replace preforms of two to three times the thickness, helping keep circuits small. Sizing of Au/Sn pads is critical and is developed from customer supplied information with respect to die size and tolerance.

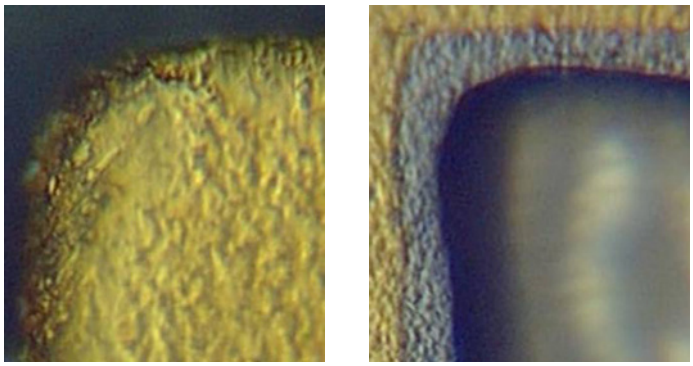


Figure 9 The image on the left shows a close up of the Au/Sn edge before reflow and the image on the right shows the Au/Sn after solder reflow.

Additionally, while Tables 17 and 18 below provide an overview of the Au/Sn material properties, we recommend a consultation with our factory for more information on available thicknesses and other details for applications and design criteria. Other solders options beyond Au/Sn are available on request.

Table 17 Au/Sn Eutectic Material Properties

Parameter	Value	Units
Composition	80 Au / 20 Sn	Wt %
Melting Temperature	284.0	°C
Density	14.5	g/cm3
Electric Conductivity	7.7	%IACS
Thermal Conductivity	57.0	W/mk
Temperature Coefficient of Expansion	16.0	m/mK
Resistivity	160.0	n ohm m
Modules of Elasticity	59.0	GPa
Tensile Strength	276.0	MPa

The eutectic material properties of the Au/Sn solder we use.

Table 18 Integrated Au/Sn (80/20 wt %) Eutectic Solder

Feature	Value	Tolerance±	Comments
Thickness range	80 - 200 µ"	20 µ"	Most common thickness = 160 µ"
Minimum feature size	.005"	N/A	
Solder pad pullback from Au metallization	.0015"	N/A	Eutectic pad is inboard of conductor
Au metallization pullback from substrate edge	.002"	N/A	Termination at edge is available, consult factory
Solder pad placement	N/A	.001"	
Minimum substrate thickness	.005"	N/A	

This table shows the properties of the integrated 80/20 Au/Sn eutectic solder we use.

Protecting Other Components in Your Circuit with Solder Masks/Dams

When using solder in a circuit, a solder mask or dam usually needs to be incorporated. This is an area of non-solderable material applied to the patterned traces of a thin-film circuit to prevent solder from flowing away from surface-mounted components during solder reflow. Unwanted solder flow can cause surface-mounted components to move during soldering or cause solder joints to be thinner and/or weak.

At Knowles Precision Devices, we offer various solder masking options to suit the subsequent processing of the substrate. Our typical options include the following:

- **TiW** – We can provide a patterned TiW layer on the conductor surface to inhibit solder flow. This method is optimum for fast, lower temperature solders to restrict run out during reflow.
- **Polyimide** – We can provide patterned polyimide as a robust solder flow restrictor. With a thickness of 7um, polyimide can withstand higher temperature solders and provides a good, robust barrier to solder flow.
- **Nickel Oxide (NiOx)** – Using our in-house plating capability, an NiOx barrier is created by etching the top surface of Au exposing an underlying layer of Ni and intentionally oxidizing the Ni. The result is an extremely robust solder flow restrictor. Note that this method requires an additional conductor layer below the Ni layer.

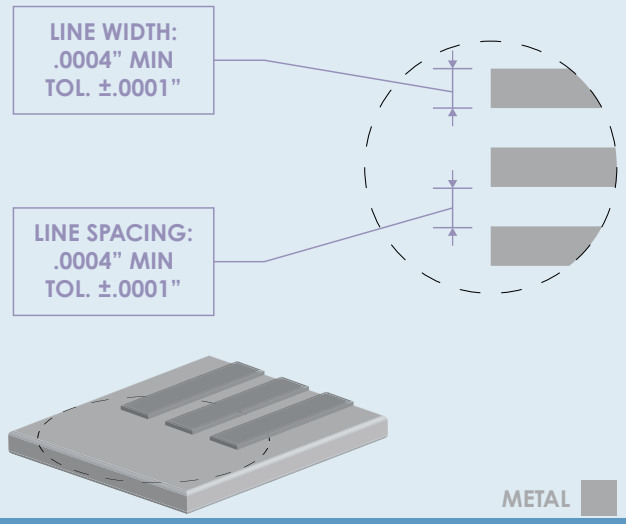
Making Connections with Supported Bridges

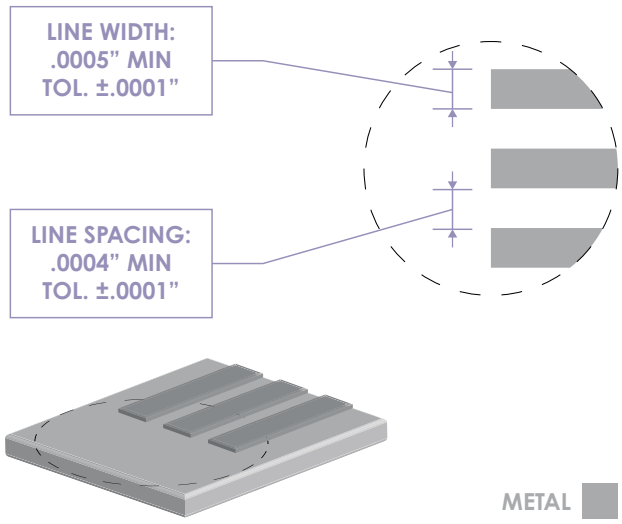
Today, many microwave circuits require the use of components such as Lange couplers to combine or split power or a spiral inductor for filtering and tuning purposes. However, when using traditional connection methods such as wire boding, these types of components can create challenges for the thin-film assembly process and are a common source of damage during manufacturing and testing. This is largely because the parasitic effects of some wire bonds make tuning and stable performance difficult, especially over broad frequency ranges.

Thus, when components such as a Lange coupler or spiral inductor are critical to a design, we use a connection option known as a supported bridge. Since we've used this method for quite some time now, we know it provides a consistent, reliable method for incorporating these structures into your designs. With supported bridges, we can also test the functionality of these components to ensure performance prior to integrating high-cost active devices. Table 19 shows the various features of our approach to creating supported bridges.

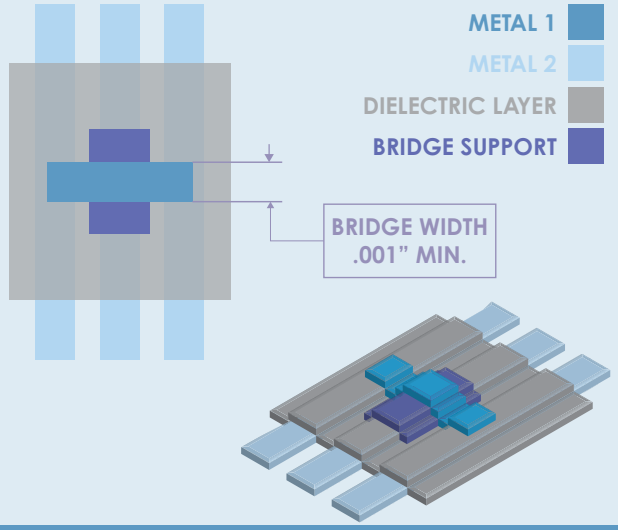
Table 19 Values and Tolerances for Our Supported Bridges

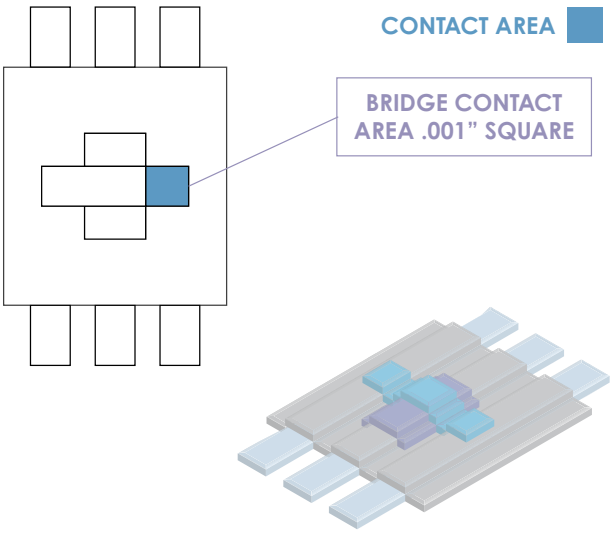
Feature	Values and Tolerances	Comments
LINE & SPACING WIDTH	.0004" minimum ± .0001"	Minimum space width available in TiW films only
LINE & SPACING WIDTH	.0005" minimum ± .0001"	Minimum line width available in TiW films only



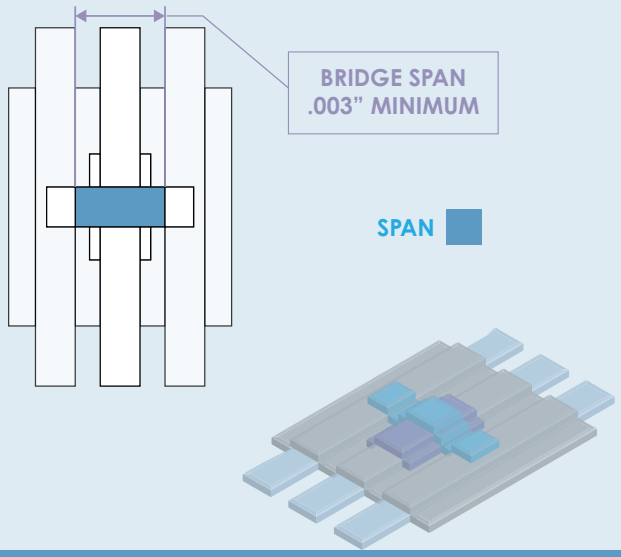


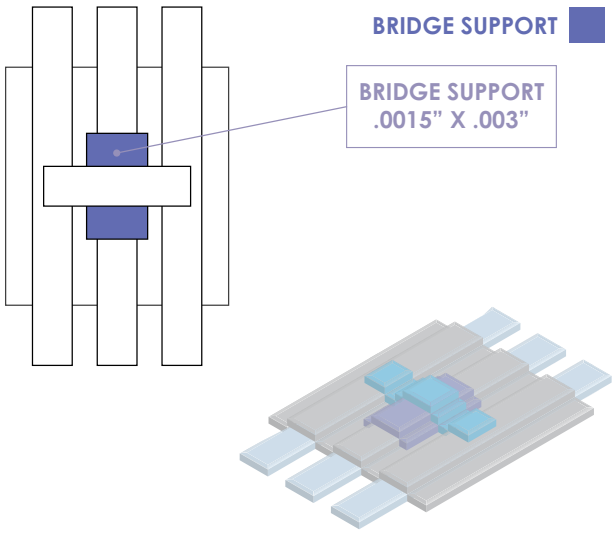
Feature	Values and Tolerances	Comments
BRIDGE WIDTH	.001" minimum	.0001" Bridge/ Conductor Pullback
BRIDGE CONTACT AREA	.001" square minimum	



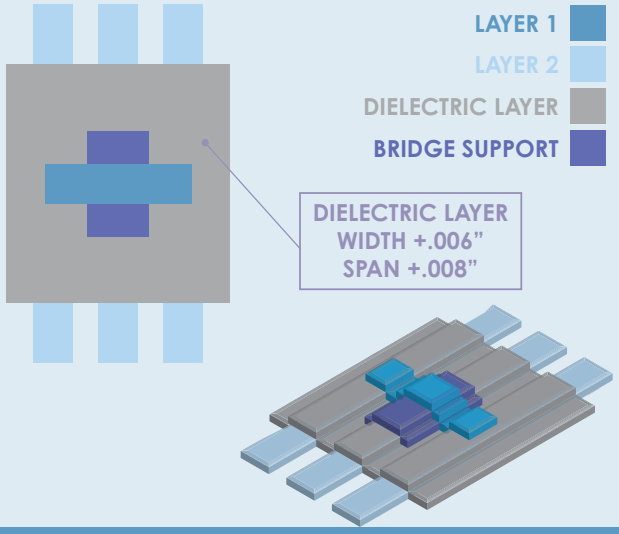


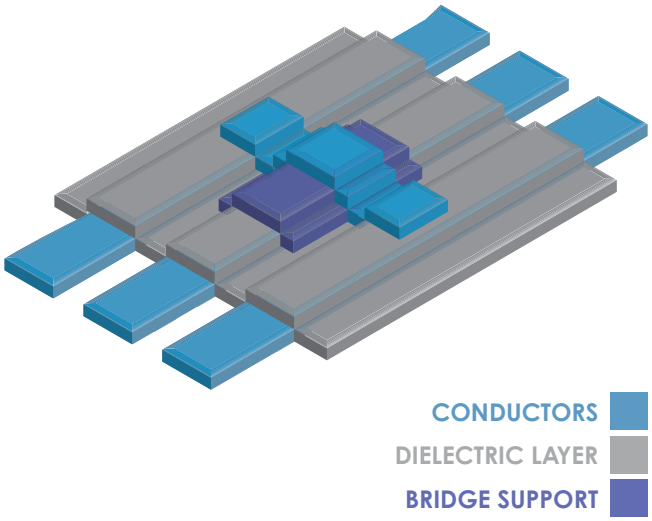
Feature	Values and Tolerances	Comments
BRIDGE SPAN	.003" minimum	
BRIDGE SUPPORT	.0015" x .003"	.0025" overlap, insulator to conductor



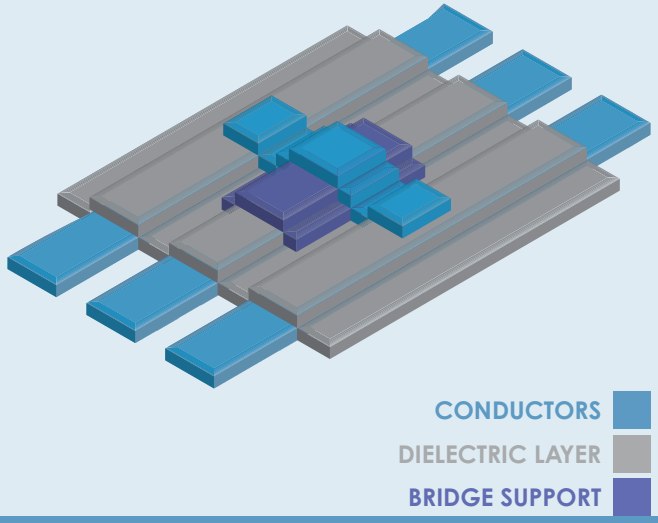


Feature	Values and Tolerances	Comments
DIELECTRIC LAYER	width + .006", span + .008"	may be deleted at factories discretion on small bridges
3D OF BRIDGE	200 microinches minimum	250 ±50 microinches typical

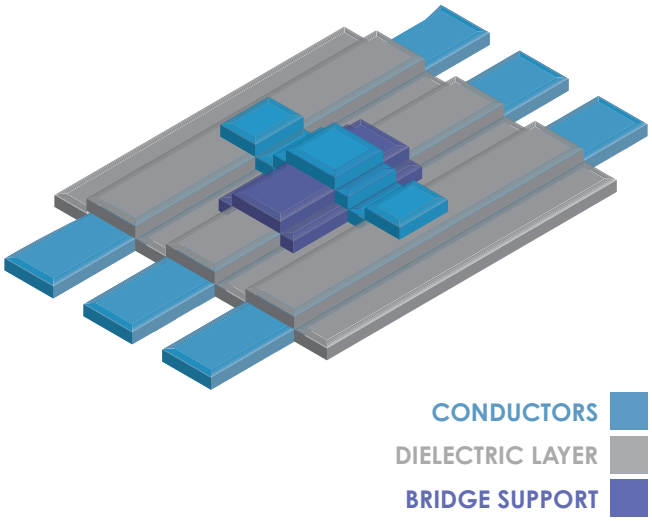




Feature	Values and Tolerances	Comments
3D OF BRIDGE	250 microinches minimum	300 ± 50 microinches typical



3D OF BRIDGE	6:1 maximum	



Custom Microwave Components

Until this point in the eBook, we've talked a lot about the processes we follow and options we make available to our customers – from substrate selection to via designs – through our build-to-print process. While it's clear we can customize basically every part of a circuit, you may be wondering, what components or devices can we actually design and develop for customers using these processes and our expertise? Let's explore the possibilities in this post.

Working with Different Types of Planar Transmission Lines

In general, our build-to-print process and thin-film technology are ideally suited for designing and building components and microwave integrated passive devices (IPDs) based on planar transmission lines, which are conductors, or in some cases dielectric strips, that are flat ribbon-shaped lines. There are several types of planar transmission line designs we can use, but for simplicity, let's focus on how we use microstrip, stripline, and coplanar waveguides for the devices we build.

First, let's look at microstrip transmission lines. These transmission lines consist of a conducting strip separated from a ground plane by a dielectric substrate (Figure 10). With microstrip technology, entire components such as antennas, couplers, filters, and power dividers are formed from metallized patterns on the substrate. By using a microstrip approach with our high K materials on high-precision thin-film photolithographic technology, components can be made lighter, more compact, and typically less expensive than what is possible with alternative transmission line technologies. This approach inherently reduces size, weight, and power (SWaP).

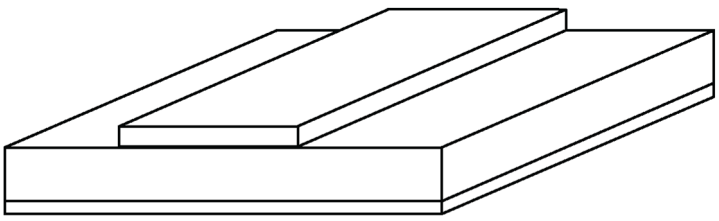


Figure 10 A drawing of a microstrip configuration.

Although stripline is similar to a microstrip approach, a stripline transmission actually lines use a flat strip of metal sandwiched between two parallel ground planes with the insulating material of the substrate forming a dielectric (Figure 11). With a stripline approach, coupled line structures do not need compensation for unequal phase velocities like those that can occur in microstrip. Also, there is less radiation using stripline, but the Q, manufacturability, and tolerance all decrease with stripline versus microstrip, which means this method is not as good of an option for applications that require higher Q and tighter tolerances.

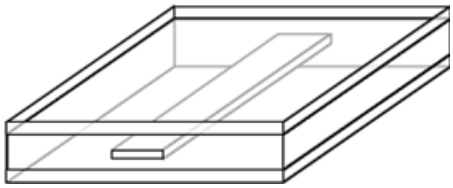


Figure 11 A drawing of a stripline configuration.

Lastly, a coplanar waveguide uses a single conducting track printed onto a dielectric substrate with a pair of return conductors on either side of the track (Figure 12). Like a microstrip configuration, coplanar waveguides can have active devices mounted on top of the circuit, although this configuration will generally not be as compact as a microstrip. Additionally, since a coplanar waveguide does not have parasitic discontinuities in the ground plane, this configuration can provide an extremely high frequency response of 100 GHz or more. This makes coplanar waveguides a good fit for monolithic microwave integrated circuit (MMIC) integrated circuit (IC) devices that operate at microwave frequencies.

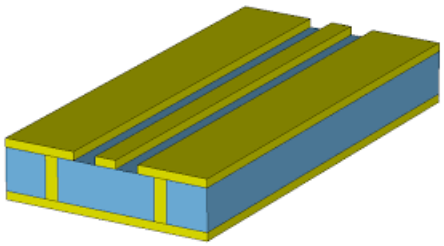


Figure 12 A drawing of a coplanar waveguide configuration.

Building Custom Microwave Integrated Passive Devices

In addition to building individual components with transmission line technologies, we also excel at building microwave and multi-stage components such as Lange couplers, Wilkinson power dividers, and hybrid bypasses. As discussed in the section on bridges and solder dams, we understand how to properly connect a variety of components using solder and connected bridges where appropriate. Thus, we can reliably integrate a variety of components such as conductors, resistors, plated vias, selective high-conductivity traces, integrated resistors, filled vias, bridges, and transmission line structures, into a single IPD. Figure 13 shows examples of some IPDs we have created for customers.

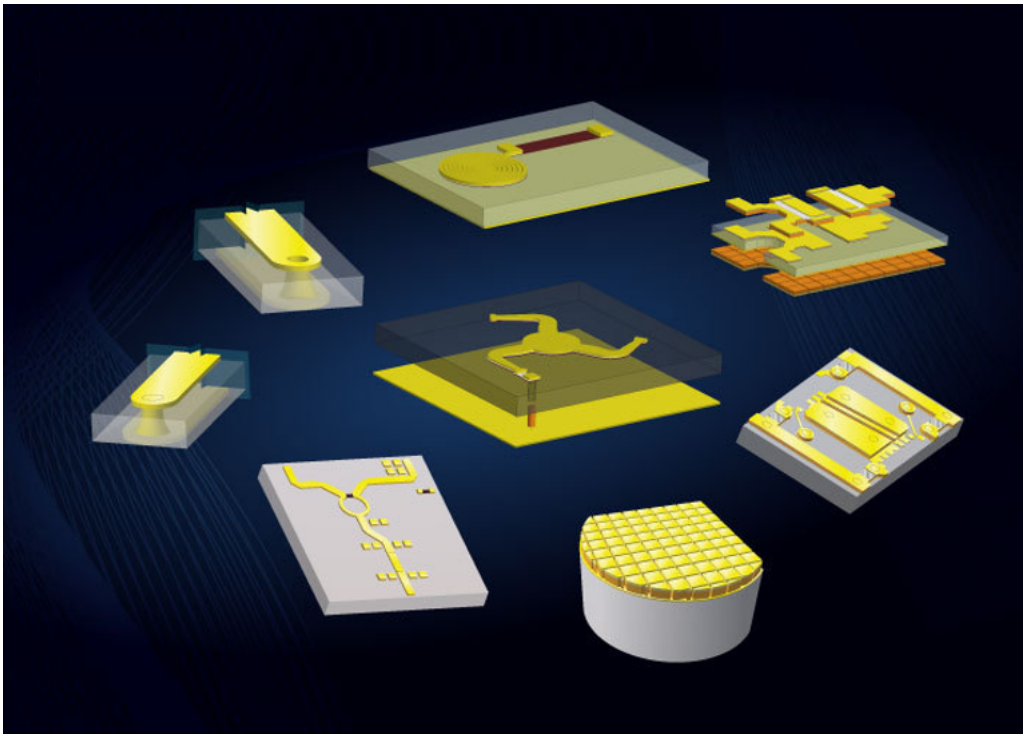


Figure 13 A sampling of IPDs, including a spiral inductor, interposer, and a power divider, that we are capable of making.

More complex integration between transmission line elements and discrete capacitor, resistors, and inductors to create IPDs is not an easy task. If this is not done correctly, condensing multiple passive components into a small device can lead to a number of issues. At Knowles Precision Devices, we excel at this. First, we offer a variety of High-K substrates that are ideal for circuit miniaturization using our thin-film process. And second, as we said earlier in this eBook, "The marriage of ceramic expertise, manufacturing know-how, product quality, customer service, product customization, and clever microwave and RF design engineering allows us to offer this variety, while many of our competitors cannot." In short, we know how to use thin film with our proven build-to-print process to make things work the way they are supposed to.

Bias Networks

In the previous section, we discussed a variety of passive microwave components, or integrated passive devices (IPDs), that we can design and develop as part of our build-to-print services. In this post, we expand on this with the details of a type of IPD, the bias network, that is commonly made with thin-film processes but used to support active microwave components such as amplifiers.

To start at the beginning, as you likely know, biasing is the process of getting DC voltage from point A to point B in the most appropriate way in a circuit. A bias network assists with this by combining capacitors and resistors in a specified way to best meet the specific needs of the device where the circuit will be used. To make a bias network, the necessary components are fabricated on the same substrate. This means that this section of the circuit can be 'abstracted' out as a single component, which saves on space and assembly cost.

Three of the most common types of bias networks are the bias filter network, the self-bias network, and the bias tee. While we can fabricate bias tees using our build-to-print process if a customer brings us a design, we mainly focus on developing bias filter networks and self-bias networks with experience frequently working all the way up to 67 GHz. Let's explore the development and functionality of these two bias networks in more detail.

Bias Filter Networks

A bias filter network can be used for biasing when it is necessary to remove noise when getting DC voltage from point A to point B in a circuit. We can design our bias filter networks for high-performance microwave applications in a surface mountable package using a combination of our temperature-stable, high-permittivity dielectrics with our thin-film processing expertise. Therefore, our bias filter networks are ideal for filtering noise from supplies and reducing RF feedback in wireless communication and high-gain RF/microwave modules. Additionally, our bias filter networks can simplify assembly and reduce the size, weight, and power (SWaP) of a circuit as one component can be used to replace many small components. An example bias filter network is shown in Figure 14.

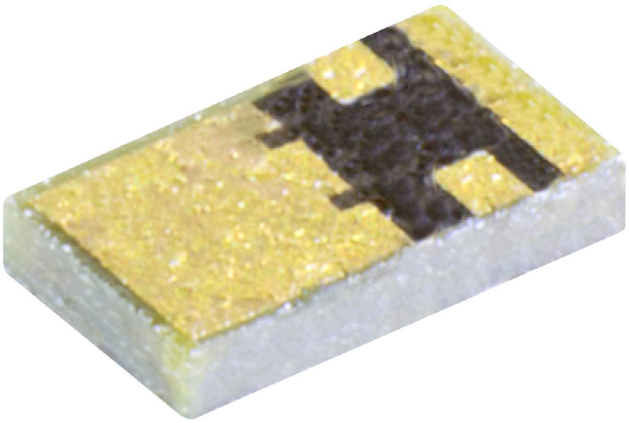


Figure 14 An example of a bias filter network we developed.

Self-Bias Networks

Self-bias networks are used to integrate source decoupling and user-selectable bias resistance. In other words, self-bias networks are used to get the current "just right" for amplifiers. To meet our build-to-print customer's needs for self-bias networks, we combine our high-permittivity ceramics with our expertise in thin-film resistors to provide a device that integrates source decoupling and user-selectable bias resistance. The self-bias networks we develop using this process can improve gain flatness and stability in GaAs field-effect transistors (FETs). Like our bias filter networks, self-bias networks can also simplify assembly since one component can be used instead of many and the SWaP of the circuit can be reduced. For example, self-bias networks used as a pair can replace two standard parallel plate capacitors and a separate set of bias resistors, reducing parts count, assembly, and size. Figure 15 shows an example of a typical self-bias network.

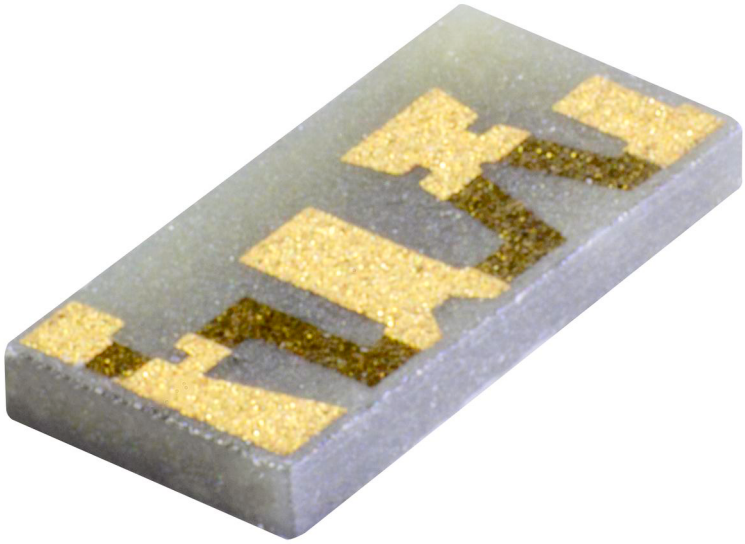


Figure 15 An example of a self-bias network we developed.

At Knowles Precision Devices, we not only have the capabilities to use thin film in the most appropriate way to develop the right bias network for your specific needs, we also have the expertise to ensure our these components are installed in a circuit in the most effective way. For example, with both bias filter and self-bias networks, we know these components should be mounted with the fully metalized side down directly on the RF ground plane for maximum isolation performance.

Testing

While any testing beyond validation testing is not a standard practice for build-to-print, since we also offer build-to-spec and custom design services in-house, our engineers are well equipped to perform a wide range of tests on our build-to-print products if needed by a customer. From basic quality tests to qualification testing to classified tests some government contractors need to comply with DD254, we offer a wide range of testing capabilities that many of our competitors cannot provide.

First, our engineering staff can create fixtures or perform wafer probing to ensure a compliant design the first time and every time in production. Additionally, our RF testing lab contains a number of thin film substrate and module test fixtures that can be configured to perform non-destructive RF tests on substrates. These fixtures are adjustable in X, Y, and Z directions and can support multiple input/output configurations.

Capabilities such as those described above can be helpful for build-to-print customers in instances where we may be producing parts that have the correct critical dimensions, yet the parts may not be achieving the performance, cost, or lead time they are looking for. In these cases, we recommend turning a build-to-print design into a build-to-spec engagement. In these engagements, beyond providing a drawing of what the part should look like, customers can provide a source control document that specifies the required RF performance. In these engagements, we then will work with the customer to adjust the build process to achieve the specifications required.

Beyond testing to achieve performance specifications, in general, if you need a specific type of test, we can get it done. From basic testing that will help improve yield or various quality aspects of your parts to secure testing for parts that use classified IP, we have the engineers and equipment in one of our two cutting-edge facilities that you may need, and the flexibility to get things done.

Military and Space Grade Applications

At Knowles Precision Devices, we know it takes high-quality and high-reliability electronic components to meet the rigorous standards required for military and space applications. After all, when launching expensive mission-critical equipment into space or using highly sophisticated electronic warfare devices to protect your citizens, there is no room for failure. Therefore, we build all our components, including those we develop for build-to-print customers, to MIL-STD-883, a standard that “establishes uniform methods, controls, and procedures for testing microelectronic devices suitable for use within military and aerospace electronic systems.”

While building to MIL-STD-883 is important for any contractor developing a part that could possibly be used in a military or aerospace application, there are likely other specifications the component must

meet as well. We are also intimately familiar with building components to a variety of other military and quality specifications, including, but are not limited to, the following:

- MIL-PRF-55681 (Group A)
- MIL-PRF-123 (Group A)
- MIL-PRF-39014 (Group A)
- MIL-PRF-49467 (Group A)
- MIL-PRF-49470 (DSCC 87106) (Group A)
- MIL-PRF-38534

We also have the capability to perform all the environmental Group B, Group C, and qualification testing the military specifications mentioned above.

Space-Ready Components

When it comes to space-qualified components, Knowles Precision Devices has proven space heritage as we've been developing space-ready components for nearly two decades. We work with a number of materials and produce various parts that are already space qualified. For example, our filled via substrates are all qualified for use in space borne microelectronic circuits. To save time and money once parts are produced, before starting a new build-to-print engagement, we encourage our customers to have a discussion with us about the materials we work with that are already approved for use in space applications.

Also, as mentioned in the testing section, we can work with customers to perform testing as needed on build-to-print parts. For example, we can perform flight screening if a customer provides a flight regimen of what testing is needed. We can also perform special life testing, sectioning, and additional electrical measurements to meet space standards such as the European Space Components Coordination Generic Specification No. 3009 (ESCC3009).

From Prototype to High Volume Production

In this ebook, we've walked through the basics of our build-to-print process and our thin-film capabilities and then broke down how we approach each of the key considerations throughout the process. We also touched on some of our additional capabilities we can offer our build-to-print customers such as testing and building components to high-reliability specifications such as those used in military and space applications. So, now that you have a better understanding of the way we work, we would love to hear from you to learn more about your application needs and how our build-to-print services may be able to address even your toughest challenges.

If you need help selecting from our portfolio please contact us and we can guide you through the selection process.

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